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EXAMINER	
LUHRS, MICHAEL K	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 04/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

SM

Office Action Summary	Application No.	Applicant(s)	
	10/774,338	BERTHOLD ET AL.	
	Examiner	Art Unit	
	Michael K. Luhrs	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *13 September 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *search history*.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species restriction in the reply filed on 1/24/2005 is acknowledged. The traversal is on the ground(s) that unconsistent description of the species. This is not found persuasive because Species II can be single (as clearly identified by lines 34-5, p. 16 of applicant's specification which the examiner cited) and Species I, multiple, as show in applicant's Fig. 14 (also cited by examiner in the restriction), hence applicant's election of species I, multiple mask layers, and claims 1-20 that applicant states read upon, is made final.

The requirement is still deemed proper and is therefore made FINAL.

Priority

2. The priority document was requested from PCT/EP by the examiner and received and subsequently entered 3/30/2005.

Specification

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and **legal phraseology** often used in patent claims, such as "means" and "said," **should be avoided**. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

a. The abstract of the disclosure is objected to because of the word "comprises", (in lines 4, 10, and 14). Such legal phraseology should be avoided. Examiner suggests replacing the word "comprises" with "includes".

b. The abstract of the disclosure is objected to because of the stray phrase "Figure 26", (in line 25).

Examine suggests removing the phrase "Figure 26", since it does not belong to the abstract.

Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claim 8 is objected to because of the following informalities: Claim 8 stipulates a thinning of the gate electrode ***prior to*** the common structuring. When considering the specification and the structuring in Fig. 14, it is

apparent that thinning occurs **after the structuring**, namely thinning occurs in Fig. 15 to 16. This seems exact opposite sequence presented by the claim. Examiner suggests changing "prior to", to --after--.

5. Claims 1 and 15 are objected to because of the following informalities:

c. Independent Claim 1 recites the limitation "mask layers" in line 2 of step "c)". There is insufficient antecedent basis for this limitation in the claim. Previous reference to mask layer is in line 3 of step "b)", yet in step "b)" "mask layer" **is not plural**. Therefore since there is no suggestion previously *using the mask layers*, in step c, the plural form lacks proper antecedent.

d. Independent Claim 15 recites the limitation "mask layers" in line 2 of step "c)". There is insufficient antecedent basis for this limitation in the claim. Previous reference to mask layer is in line 3 of step "b)", yet in step "b)" "mask layer" is not plural. Therefore since there is no suggestion previously *using the mask layers*, in step c it lacks proper antecedent.

6. Appropriate correction is required.

Double Patenting

7. Claims 1-20 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 17-20 of copending Application No. 10/774,349. Although the conflicting claims are not identical, they are not patentably distinct from each other because they claim similar subject matter in that the fabrication operation of step b) (second occurrence) of claim 17 of 10/774,349 as to fabrication of structuring in independent claims 1 and 15 of the present application.

8. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 1, 2, 3, 6, 9, 12-13, and 15, 17,18 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Sawada et. al. USPN 6,001,676.

Regarding claim 1, Sawada et. al. teach *a) generating a MOS preparation structure in the MOS area, wherein the MOS preparation structure comprises an area provided for a channel, a gate dielectric, a gate electrode layer and a mask layer on the gate electrode layer*; as, MOS area (2) and (3) and bipolar area (1) as seen in Fig. 2 in epitaxially layer 11, on wafer 10 (line 49, column 11 through line 5, column 12) with 13A collector region for bipolar area (1) as seen in Fig. 3 as discussed in line 7, column 12, n-well 13B and p-well 14B is in epitaxial layer 11 as discussed in lines 8-15, column 12, and oxidation to provide gate insulator (dielectric) 16C and D, in lines 45-47, column 13, Fig. 3, and the gate electrode 18C and D, lines 52-53, column 13, in Fig. 4, the channel is located under the gate dielectric 16C and D, between source and drain areas 27A and 28A of MOS's (2) and (3), as these areas are doped as seen in Fig. 7; the mask is a photoresist mask, not shown, but described in lines 26-30, column 14 is on the electrode i.e. to form 18A,C and D, see lines 30-31, column 14,

Sawada et. al. teach *b) generating a bipolar preparation structure the bipolar area, wherein the bipolar preparation structure comprises a conductive layer and a mask layer on the conductive layer;* as polysilicon layer is used to form 18A and 18C and D of the MOS (lines 49-50, column 13, see especially the polysilicon in lines 5-6, column 14) in Fig. 4, the mask layer as a photoresist, cited above, is on this polysilicon,

step c) common structuring of the gate electrode layer and the conductive layer by using the mask layers[sic] *for defining a gate electrode in the MOS area and a base terminal area and/or emitter collector terminal area in the bipolar area* by structuring, using a photoresist pattern (line 27, column 14) in bipolar 16A and same mask as to structure the MOS gates, see Fig. 4, this preparation structure also includes an insulation layer of TEOS 19A (line 22-23, column 14) over the bipolar area and as 18C and D over the MOS (TEOS is on each electrode (lines 48-50, column 9) hence commonly structured, 18A,C and D, and even the opening 17 for the NPN bipolar is formed, (lines 35-38, column 17).

Sawada et. al. teach *d) simultaneous generating of isolating spacing layers on side walls of the gate electrode layer in the MOS area and the conductive layer in the bipolar area by depositing a first and second spacing layer, wherein the isolating spacing layers serve for defining areas to be doped in the MOS area and the first spacing layer serves for isolating a base area and an emitter area in the bipolar area*; as isolation spacing layer namely,

oxide 20A, C, and D, in Fig. 5 (line 46, column 14) as well as 21A, C and D nitride layer (line 65, column 14) (first spacer) and polysilicon: 22A, B and E and F (lines 3-5, column 15) (i.e. second spacer), doping occurs in lines 19-42, column 16 using the nitride 21C and D; spacers 20A and 21A serve to provide isolation to region 17 in Fig. 5 from the base layer 18A originally provided and structured; examiner also points out that another spacer is included later, as spacers 29A and B used to for optimization as seen in column 17 lines 21+ to dope the MOS illustrated in Fig. 7.

Sawada et. al. teach a*nd e) selective etching of the first spacing layer and the second spacing layer in the MOS area and the bipolar area;* by etching the oxide/polysilicon /nitride discussed above, first etching anisotropically (line 17-18, column 15) then (as in lines 25-39, column 15) is an etch of the polysilicon as a mask to form the nitride against the sides of the electrodes 18A, C and D, for openings as location 33, for bipolar region (1) in Fig. 3 (as well as aside the MOS gates in regions (1) and (2)).

And, Sawada et. al. teach, *f) removing the second spacing layer in the MOS area and the bipolar area.* Sawada et. al. teach this in column 16 regarding the stripping of the polysilicon, see that Sawada does in fact remove the polysilicon layer (Sawada's layer 22E is removed from Fig. 5 to Fig. 6) as well as in the emitter region as discussed explicitly in lines 63-64, column 16, hence the second spacer is removed.

Regarding claim 2, *re: the Method according to claim 1, wherein the mask layer in the MOS area and the mask layer in the bipolar area is generated by common depositing of at least one isolation layer.* It is clear that spacers 20A, 21A and 22A isolate 18A in the bipolar area (1) into two regions separated by opening 33, an addition layer (29A) line 66, column 16 and line 28, column 17, isolates between the bipolar area and the MOS in Fig. 7 and yet also the TEOS layer (19A, C and D) in Fig. 4 isolates the base from the emitter electrode.

Regarding claim 3, the photoresist patterning of line 25-26, column 14 is used to structure the layer 18A and the TEOS therefore Sawada et. al. teach the. *Method according to claim 2, which further comprises the step of structuring the mask layer in the MOS area for defining the gate electrode and in the bipolar area for defining the base terminal area and/or collector area.* Because the bipolar and MOS areas are structured by dry etch (line 26, column 14) and etching anisotropically (line 29, column 14) the TEOS and polysilicon layers, respectively.

Regarding claim 6, Sawada et. al. teach the bipolar and MOS areas are structured by dry etch (line 26, column 14) and etching anisotropically (line 29, column 14) the TEOS and polysilicon layers discussed above, whereas the

polysilicon layer is in fact, used to form 18A of the bipolar device, and the gate (or *at least part of* Applicant's claim language in italics) the gate of the MOS, in fact, it is the whole gate of the MOS device, and this polysilicon is a common deposition on the entire surface as expressed in lines 6-7, column 14.

Regarding claim 9, Sawada et. al. teach photoresist pattern (in line 56, column 14) for ion implantation of base region 35 (line 60, column 14).

Regarding claim 12, Sawada et. al. teach the doping of 27A and 30A (seen in Fig. 7) occurs after the structuring, of Fig. 4.

Regarding claim 13, Sawada et. al. teach that the formation of the gate and layer for the bipolar is simultaneous because they are commonly structured, 18A,C and D, and even the opening 17 for the NPN bipolar is formed, (lines 35-38, column 17), is at the "same time" (as explicitly stated, in line 37, column 14), i.e. same etching.

Regarding independent claim 15: since claim 15 is a combination of the limitations already addressed above for claims {1, 2 and 6}, the same citations apply to claim 15, please refer back to them.

Regarding claim 17, imparting the same limitations as presented in claim 9 (namely, the window disposed,), already addressed above, please refer back to these citations.

Regarding claim 18, imparting the same limitations as presented in claim 10 (namely the structuring of collector/emitter), already addressed above, please refer back to these citations.

Regarding claim 20, imparting the same limitations as presented in claim 12 (namely the doping), already addressed above, please refer back to these citations.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time

any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

13. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et. al. as applied to claim 1, above, in further view of Miwa et. al. 5,662,887.

Sawada et. al. does not discuss any additional devices constructed in parallel. Miwa et. al. show construction of a MOS capacitor (i.e. MIS C) Fig. 12 left side, in conjunction with the NPN and MOS's, right side, i.e. these devices can be constructed on the same substrate for circuitry that require them. Therefore it would have been obvious at the time the invention was made to one having ordinary skill in the art that parallel generation of one or several devices of the group varactor and MOS capacitor, could be made in parallel, since Miwa et. al. explicitly recognize the construction of the MOS capacitor with the NPN and MOS's in Fig. 12, i.e. Miwa et. al. are especially presenting the capacitor with the polysilicon to replace the metal electrode is thus making the capacitor structure more friendly to the other devices by providing the capacitor electrode and bipolar electrode of the same material at the same time.

14. Claims 11 and 19 rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et. al. as applied to claims 1 and 15 respectively, above, in further view of Schafbauer et. al. USPN 6,815,317.
Sawada et. al. fails to provide the ARC (antireflective coat) to their photoresist masking. Schafbauer et. al. teaches that ARC is beneficial for defining the emitter and gate of MOS. It would have been obvious at the time the invention was made to one having ordinary skill in the art to utilize the ARC as recognized by Schafbauer et. al. to facilitate the construction of the emitter and gate of MOS with the benefit it provides when ion implanting is involved.

Allowable Subject Matter

15. Claims 4, 5, 7, 8, 10 and 11 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim (and objection thereto) and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: Re: claim 4, the thinning of the mask layer in the area of the gate electrode was not suggested by the prior

art. Re: claim 5, the wherein the mask layer comprises a first and second isolation layer was not suggested by the prior art. Re: claim 7, the *first and second parts* of the gate electrode, wherein the second part is [also] deposited with the [as] the conductive layer for the bipolar area was not suggested by the prior art: i.e., Sawada et. al. teach that the polysilicon is commonly deposited yet the gate does not have the two parts suggested by the claim. Re: Claim 8, the examiner considers the allowable matter for the thinning *after* (please see the objection for claim 8) the common structuring, as suggested by the specification, was not found or suggested in the prior art. The examiner also considered *prior to* as indicated by applicant's presently presented claim language. The "prior to" sequence is also allowable matter. The thinning of the gate electrode *prior to* the common structuring was not suggested by the prior art; (this is the same reasoning for claim 16, hence claim 16 also has this allowable matter.) Re: Claim 10, Sawada et. al. teach the polysilicon deposited in line 5-6, column 14, is in fact the conductive layer in the areas of the bipolar region, yet puts down the electrode 26 for collector much later, hence the electrode 26 common formed with the conductive layer for the transistor is allowable matter. Re: claim 11, the generation of antireflection layer on the mask was not suggested by the prior art.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.. Tsubone et. al. USPN 5,100,815 has applicant's simultaneous construction but lacks the second spacer removal. Examiner considered carefully applicant's IDS submitted September 13, 2004, of which EP 0 746 032 A2 clearly provides common structuring and spacing layers of Fig. 4 to Fig. 5.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael K. Luhrs whose telephone number is 571-272-1874. The examiner can normally be reached on M-F, 8-5.

18. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

19. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MKL

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4/7/05

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